Charge Pump PLL Modeling

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Based on Extending Work Done in 1991-1992

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Glossary

Abbreviation	Description
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
Capsim	Hierarchical Block Diagram C Simulator
VCO	Voltage Controlled Oscillator
DBN	Divide by N
CHP	Charge Pump

Introduction

The high level block diagram of the PLL is shown in Figure 1. It is imperative to have a high level behavioral model of the PLL in Capsim in order to verify the operation of the PLL and to do extensive "what if" scenarios and fine tune the design parameters.

A block diagram level simulator was written in C which allows for very fast simulations and the verification of PLL performance. This is based on a Capsim phase-frequency detector and charge pump block diagram simulation by the author's Ph.D. Student, Ray Kassel in 1990 at NC State University. See http://www.silicondsp.com/Capsim.

The preliminary goal is to match the nonlinear mixed analog/digital PLL circuit in terms of predicting overall performance.

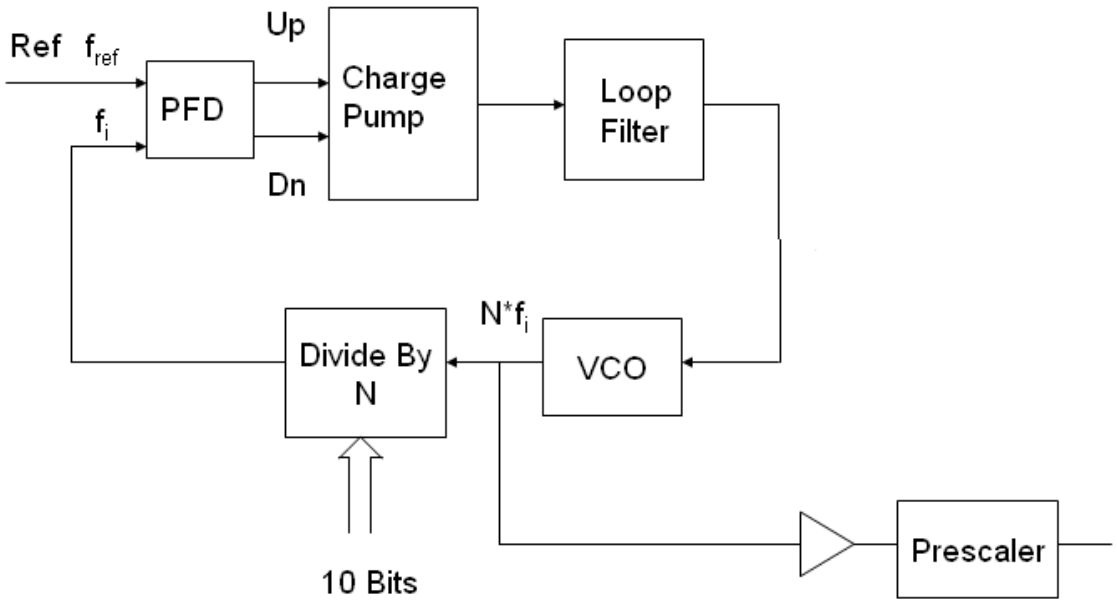

Figure 1 High Level Block Diagram of PLL Synthesizer

Capsim Model Architecture

For the Capsim simulation, a time increment is defined and time is advanced until a predefined simulation time is reached. For reasons that will be explained later the time increment will be very small. We use 1ps as the time step yet achieve very fast simulation time.

In Capsim we can plot the various nodes and also dump the signals to files for post processing and display. Post processing is very important. In particular we have used a program to compute the timing jitter between the reference clock and the PLL clock. The jitter is used to verify performance and to observe how the PLL responds to events and VCO phase noise among other parameters.

In order to verify and tune the design a Capsim simulation of a charge pump synthesizer was carried out. The topology is shown below. The reference clock is 4 MHz. The VCO center frequency is 1 GHz. The charge pump is setup with current of 1 uA, Rp=5000 Ohms and C1=10 pF. More on this later. The simulation results are shown.

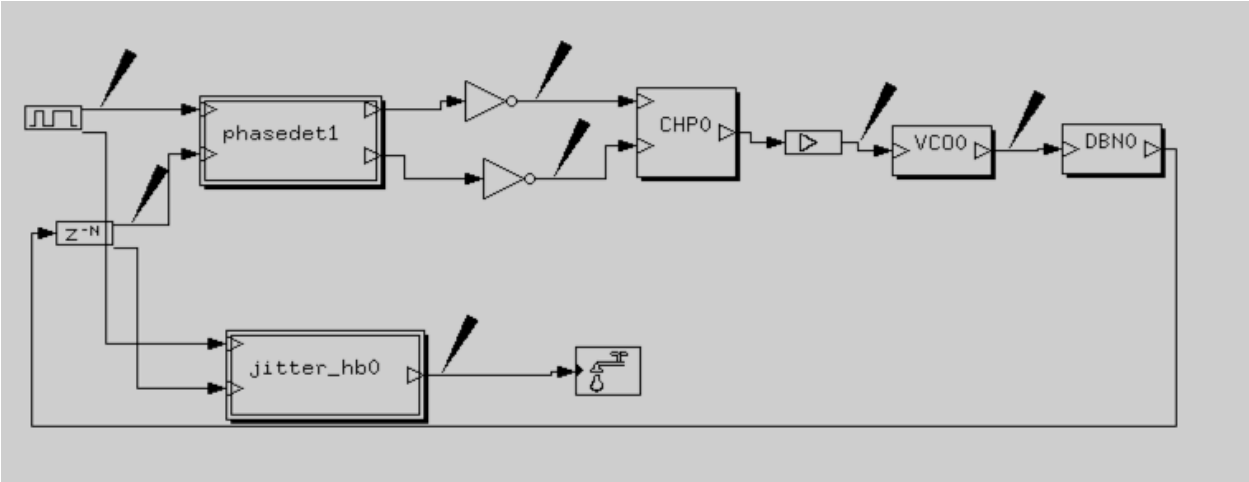

Figure 2 Capsim Block Diagram of Charge Pump PLL

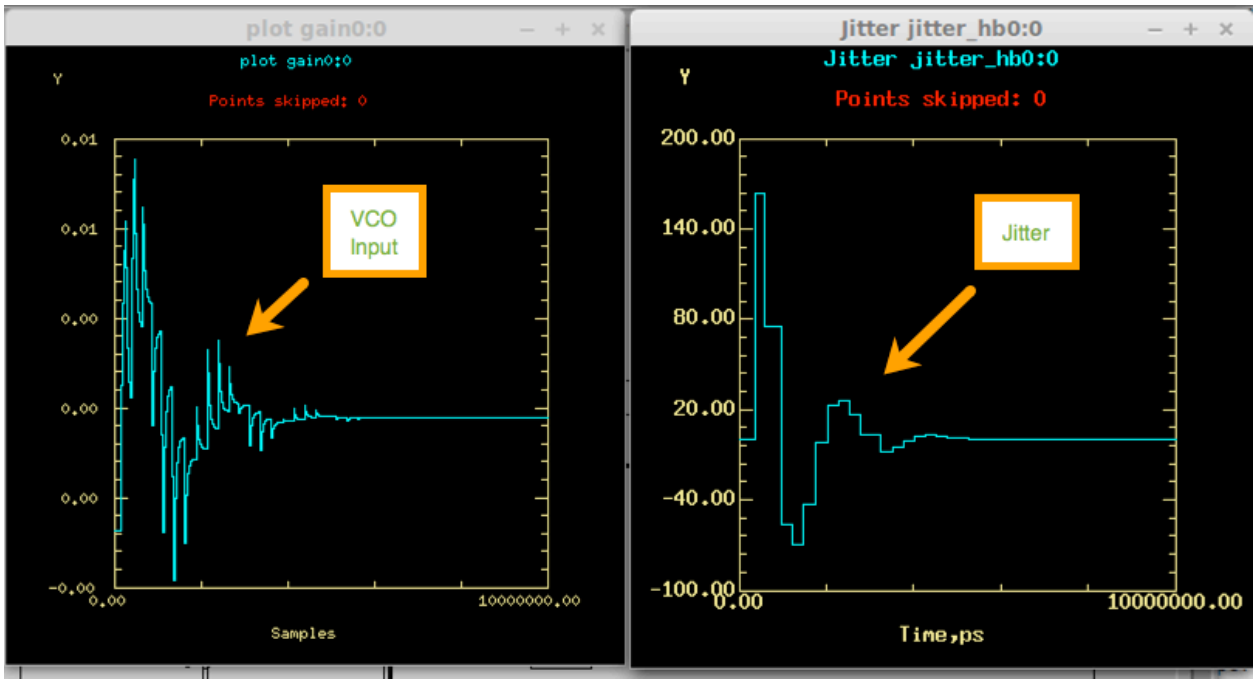

Figure 3 Charge Pump PLL Simulation Showing Error Signal (input to VCO) and Measured Jitter

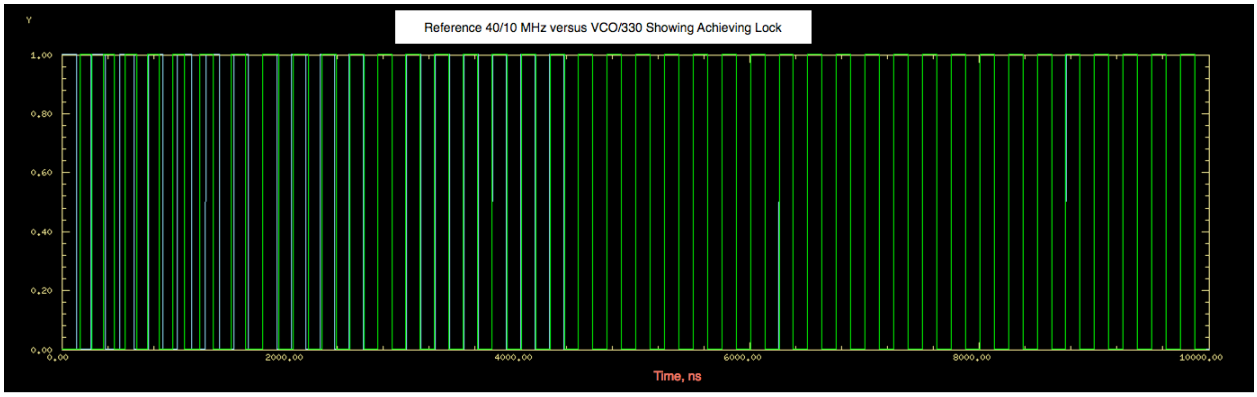

Figure 4 Grouped Plot with Reference 4MHz (40/10) and VCO/330 Showing Lock Achieved.

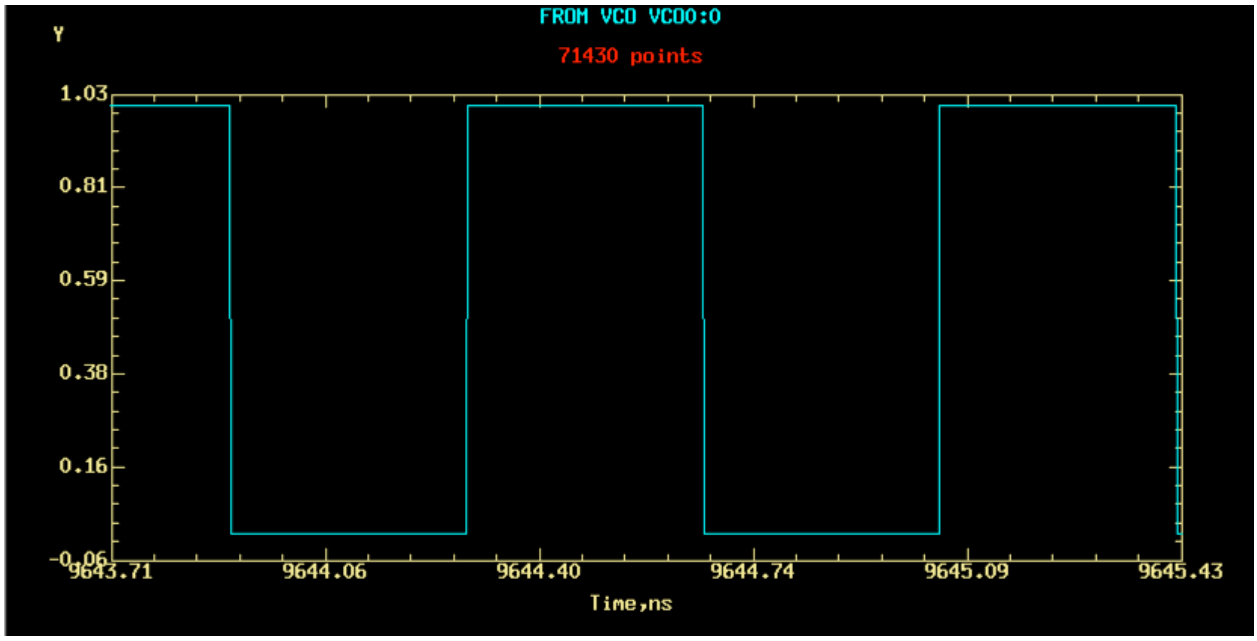

Figure 5 Frequency Measured at 1.32 GHz from Period

Modeling the Charge Pump

A key requirement for the Capsim high level model is to accurately capture the PLL behavior with the correct modeling of the charge pump.

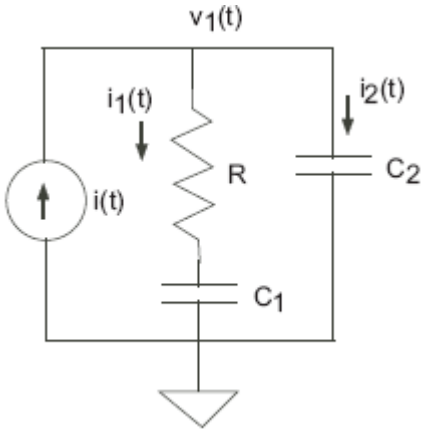

Figure 6 Charge Pump During Up Cycle

These equations are valid for very short time intervals. In order to verify these equations, the continuous time solutions based on a state space formulation, derived in [1], were coded in C and integrated into the Capsim high level block model. See Appendix A for these equations.

Timing Jitter Measurement in Capsim High Level Model Simulation

A key figure of merit for the performance of the PLL clock synthesizer is the timing jitter of the synthesized clock with respect to the reference. The Capsim Behavioral program stores various nodes into files for post processing. A Capsim Block Diagram for Jitter Measurement reads in the stored reference and the VCO signal after divide by N and measures the timing jitter. A key requirements for the design of a clock synthesizer are specified in terms of the rms jitter.

PLL Synthesizer Stability

The charge pump PLL can go unstable under certain conditions. We will not present a full analysis here but will explain the cause of instability. For a full development see [2]. The charge pump PLL with Phase Frequency detector is a mixed continuous and sampled nonlinear feedback system. Consider the case where we are in the tracking mode (where phase errors are small). The Reference signal in the PFD acts as a sampling signal at the reference frequency. If the block diagram in terms of the phase is modeled in the Z-domain (for sampled systems), then a root locus analysis shows that as the loop bandwidth increases (related to loop gain), the system can go unstable. In fact, if the clock frequency of the reference is very high compared to the loop bandwidth, then the Charge Pump PLL can be modeled as a continuous system. And if we neglect the smoothing capacitor (C2) assuming C1>>C2, then the PLL can be modeled as a second order PLL and it is always stable for various loop gains (bandwidth). In fact many aspects of the dynamic behavior of the charge pump PLL can be accurately predicted using an s-domain analysis and treating the PLL as a continuous system. See Appendix B. As we mentioned this holds true if the reference clock frequency is much higher than the loop bandwidth.

However, as the reference frequency is decreased, then the continuous time model is invalid and instability can result (note that at lower reference clock frequencies a z-domain delay becomes significant to the phase margin which can cause instability).

The Caspim block diagram model of the PLL is well suited for stability analysis and to verify that the PLL is stable. Also the Capsim model can be used to gain confidence in the validity domain of the various theoretical design equations for the charge pump PLL.

To check the theory against the Capsim model, we will predict at what Reference frequency the PLL is unstable and then check the Capsim model to see if the PLL goes unstable for these parameters.

According to the theory [2], the charge pump PLL should approach instability under the following conditions:

- Ref= 40MHz
- C1=2pF,C2=0.2pF,R=1KΩ, Ip=50uA
- N=16
- Calculated BW =7.1 MHz
- REF not >> than BW unstable.

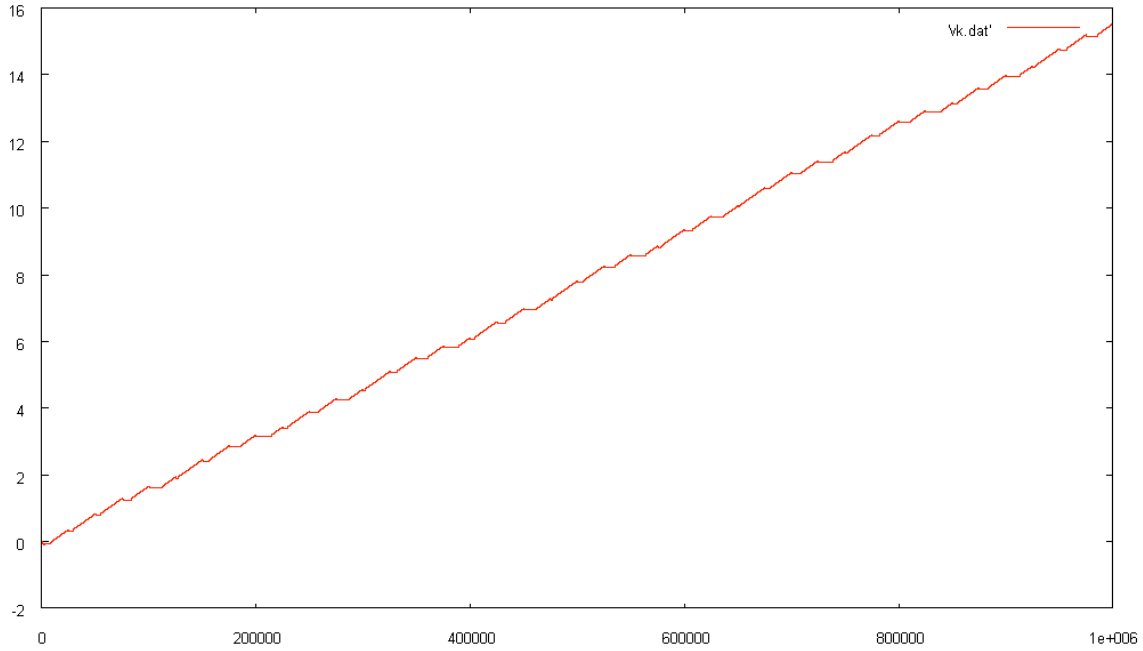

Figure 7 VCO Input from Capsim Model Showing Instability at Low Reference Clock Frequency

Table 1 shows the range of stability for various Reference Clock frequencies.
Figure 7 shows the VCO input which indicates instability at 40MHz reference frequency.

Table 1 Stability versus Reference Clock Frequency

Reference MHz	K_{stable}, Hz	K/K_{stable}
16	1924812	3.689853
20	2962963	2.397017
30	6428571	1.104798
40	11034482	0.643643
50	16666666	0.426136
60	23225806	0.305792
70	30624999	0.231911
80	38787878	0.183105
90	47647058	0.14906
100	57142856	0.12429
110	67222220	0.105654

PLL Bandwidth and RMS Jitter

The interplay between PLL bandwidth and reduction of jitter in the synthesized clock due to both phase noise in the VCO and noise injected into the control signal of the VCO is examined. We will start by showing simulation results of the measured clock jitter due to noise injected in the VCO control signal as shown in Figure 8.

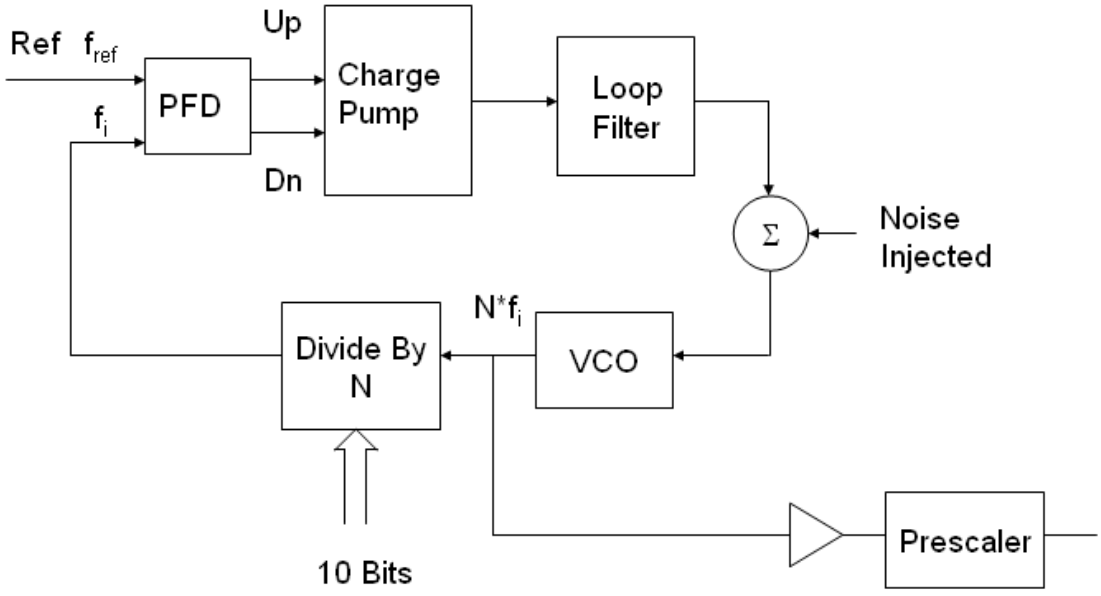

Figure 8 Noise injected into VCO control signal

Figure 9 shows the clock jitter for noise with variance 0.001 injected into the VCO control voltage for C1=10pF, C2=1pF, and R=1kΩ.

In the following we will increase the PLL Bandwidth by increasing the resistance R_1. The PLL bandwidth can be defined in terms of the loop gain:

$$K = \frac{K_0 I_p R_1}{2\pi N}$$

Where K_0 is the VCO gain, N is the divide by N counter setting, I_p is the charge pump current, and R_1 is the charge pump filter resistance (R in Figure 6).

Figure 9 shows the zoomed in jitter for R_1=1kΩ. As we increase R_1 to 5kΩ the jitter is significantly reduced as show in Figure 10.

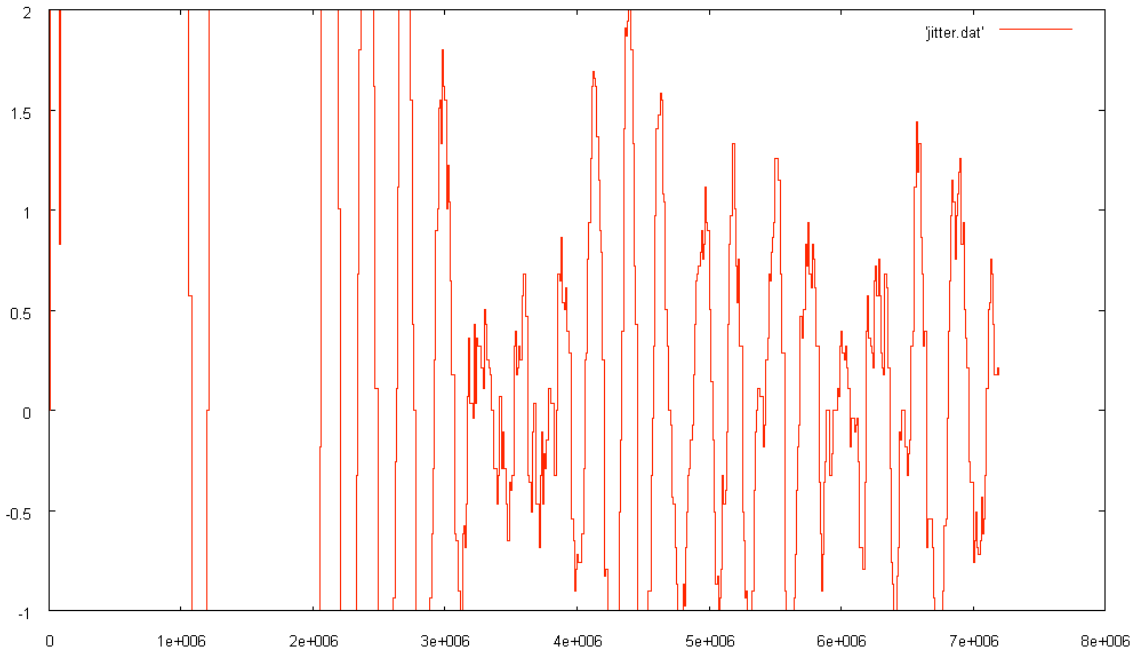

Figure 9 Jitter C1=10pF C2=1pF R=1kΩ Noise Variance=0.001 Zoomed In Time in ps.

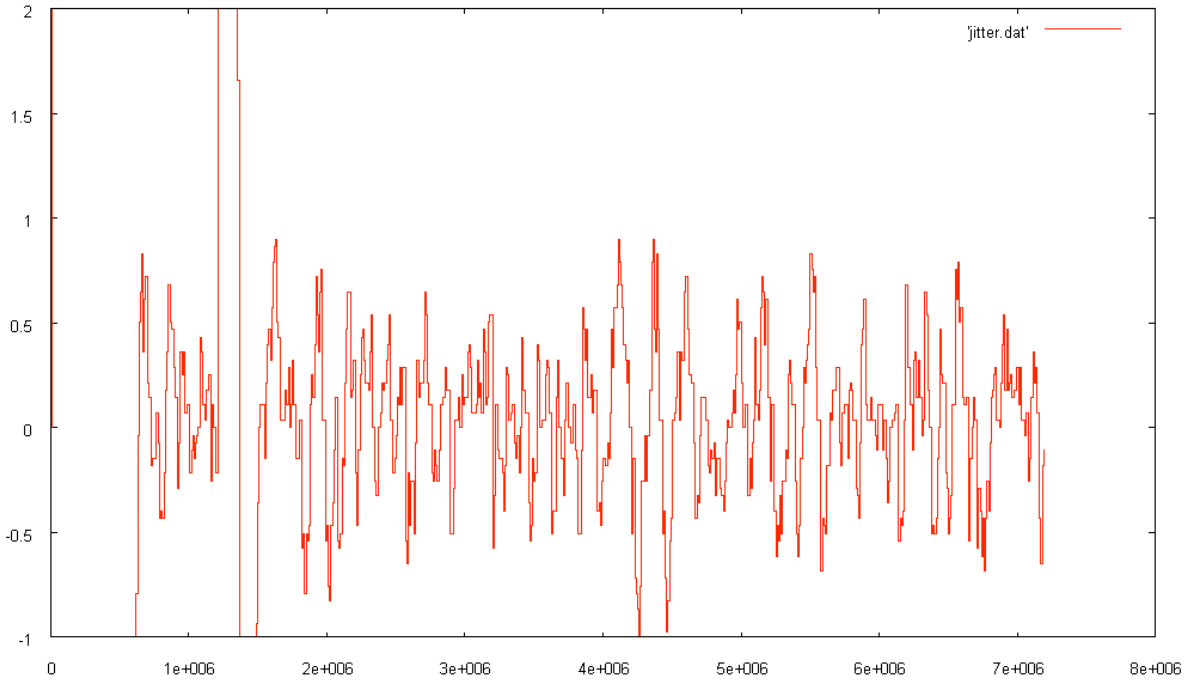

Figure 10 Jitter C1=10pF C2=1pF R=5kΩ Zoomed in, Time in ps.

Theoretical Results for Timing Jitter

In the literature [3] and [4], the effect of phase noise in the VCO on the synthesized clock jitter has been analyzed. The jitter due to noise injected at the VCO control signal and phase noise of the VCO both decrease with increases in the bandwidth. There are differences, however. The results we show here are for the rms jitter due to phase noise. For noise injected in the VCO control signal and phase noise, increasing the bandwidth through increasing R_1 and or I_p decrease the rms jitter.

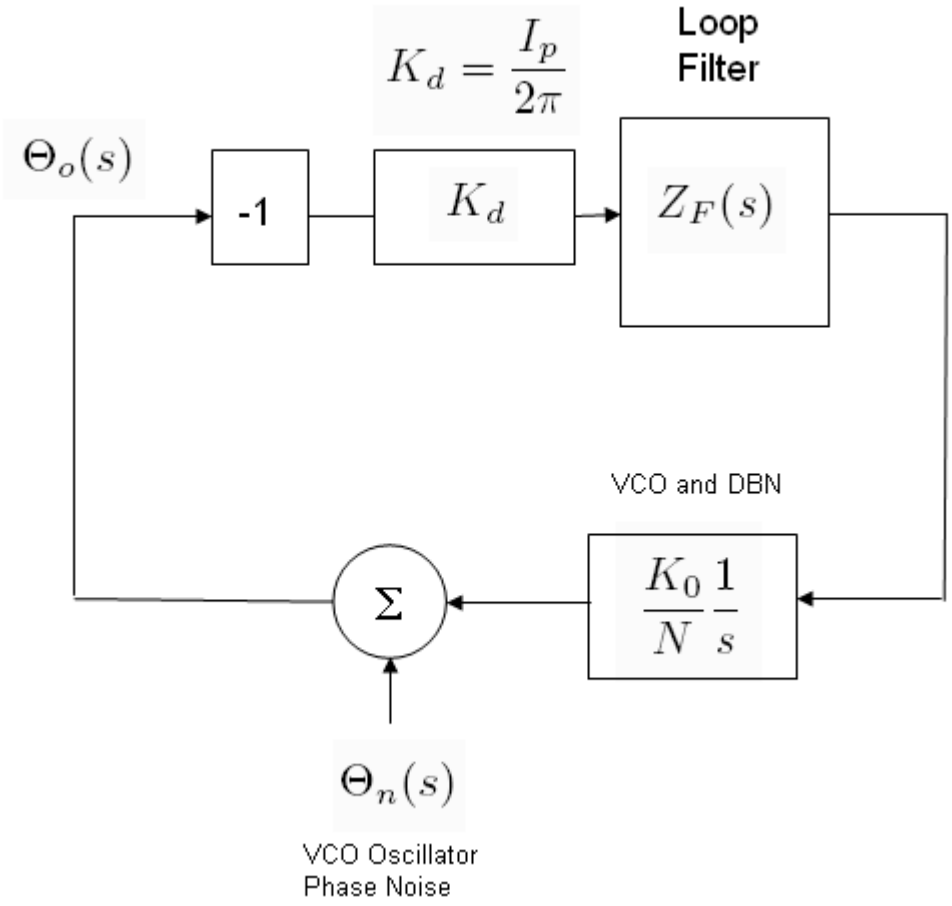

Figure 11 Phase Noise Due to VCO

According to [3] the rms jitter in the synthesized clock is given by the expression below:

$$\sqrt{E[\Theta_{tot}^2(nT)]} = \sqrt{\frac{1}{2K_L T}} \frac{2\pi\Delta\tau_{rms}}{T}$$

where,

$$K_L = \frac{K_0 I_p R_1}{2\pi N}$$

and

T Reference Clock Period.

The VCO jitter due to phase noise is expressed by $\Delta\tau_{rms}$.

We observe that by increasing the loop gain K_L which is equivalent to increasing the PLL bandwidth, we decrease the rms jitter in the synthesized clock.

Note that for clock recovery applications, we are generating a stable clock from a noisy signal and using the transitions in the data. In this case, we require a small bandwidth to reduce the jitter in the recovered clock. For this application we are looking at the transfer function from the input phase $\theta_i(s)$ to the output phase $\theta_O(s)$. In the case of a clock synthesizer we are looking at the transfer function between the VCO phase noise $\theta_n(s)$ and the output phase, $\theta_O(s)$. Refer to the block diagrams in Figure 1 and Figure 11 and Figure 15 (Appendix B).

References

[1] Hanumolu, P.K.; Brownlee, M.; Mayaram, K.; Un-Ku Moon,**"Analysis of charge-pump phase-locked loops"**, Circuits and Systems I: Regular Papers, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Volume 51, Issue 9, Date: Sept. 2004, Pages: 1665 – 1674

[2] Gardner, F., **Charge-Pump Phase-Lock Loops**, IEEE Transactions on Communications, Volume 28, Issue 11, Date: Nov 1980, Pages: 1849 – 1858. Also see Gardner's Text Book on PLL's.

[3] Beomsup Kim; Weigandt, T.C.; Gray, P.R., **PLL/DLL system noise analysis for low jitter clock synthesizer design** *IEEE International Symposium on Circuits and Systems*, 1994. ISCAS '94., 1994 Volume 4, Date: 30 May-2 Jun 1994, Pages: 31 - 34 vol.4

[4] Kyoohyun Lim; Seunghee Choi; Beomsup Kim **Optimal loop bandwidth design for low noise PLL applications** *Proceedings of the Design Automation Conference* 1997. ASP-DAC '97. Asia and South Pacific Date: 28-31 Jan 1997, Pages: 425 - 428

Appendix A

In the following from [1], v_{ctrl} is v_1. and v_c is v_2 across C_2. t_p is the on time of Up or Down pulse. T_ is related to the period of the reference or the next edge of VCO/N. That is the time $t_p<t<T\_$ is the off time of the Up or Down pulse. See Figure 12.

$$\text{for } 0 < t \le t_p$$

$$v_{\text{ctrl}}(t) = v_{\text{ctrl}}(0)\left(g_1(t) + \omega_z g_2(t)\right) + v_c(0)\omega_2 g_2(t) + \frac{i_p}{C_2}\left(g_2(t) + \frac{\omega_z(g_1(t)-1)}{\omega_{p3}^2} + \frac{\omega_z t}{\omega_{p3}}\right)$$

$$v_c(t) = v_{\text{ctrl}}(0)\omega_z g_2(t) + v_c(0)\left(g_1(t) + \omega_2 g_2(t)\right) + \frac{i_p}{C_2}\left(\frac{\omega_z(g_1(t)-1)}{\omega_{p3}^2} + \frac{\omega_z t}{\omega_{p3}}\right)$$

$$\text{for } t_p < t \le T\_$$

$$v_{\text{ctrl}}(t) = v_{\text{ctrl}}(t_p)\left(g_1(t) + \omega_z g_2(t)\right) + v_c(t_p)\omega_2 g_2(t)$$

$$v_c(t) = v_{\text{ctrl}}(t_p)\omega_z g_2(t) + v_c(t_p)\left(g_1(t) + \omega_2 g_2(t)\right).$$

In the above, $\omega_2 = 1/RC_2$, $g_1(t) = \exp(-\omega_{p3}t)$, and $g_2(t) = (1/\omega_{p3})(1 - \exp(-\omega_{p3}t))$.

$$\omega_z = \frac{1}{RC_1}$$

$$\omega_{p3} = \frac{1}{R\left[\frac{C_1 C_2}{C_1 + C_2}\right]}$$

$$\omega_2 = 1/RC_2$$

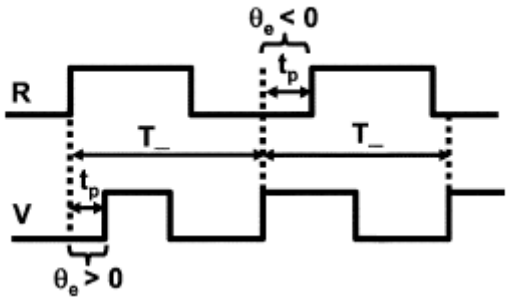

Figure 12 Definition of t_p ad T_ from [1].

In the above note that all the exponentials are based on e^{-at}, where, as we derived before:

$$a = \frac{C_1 + C_2}{RC_1C_2}$$

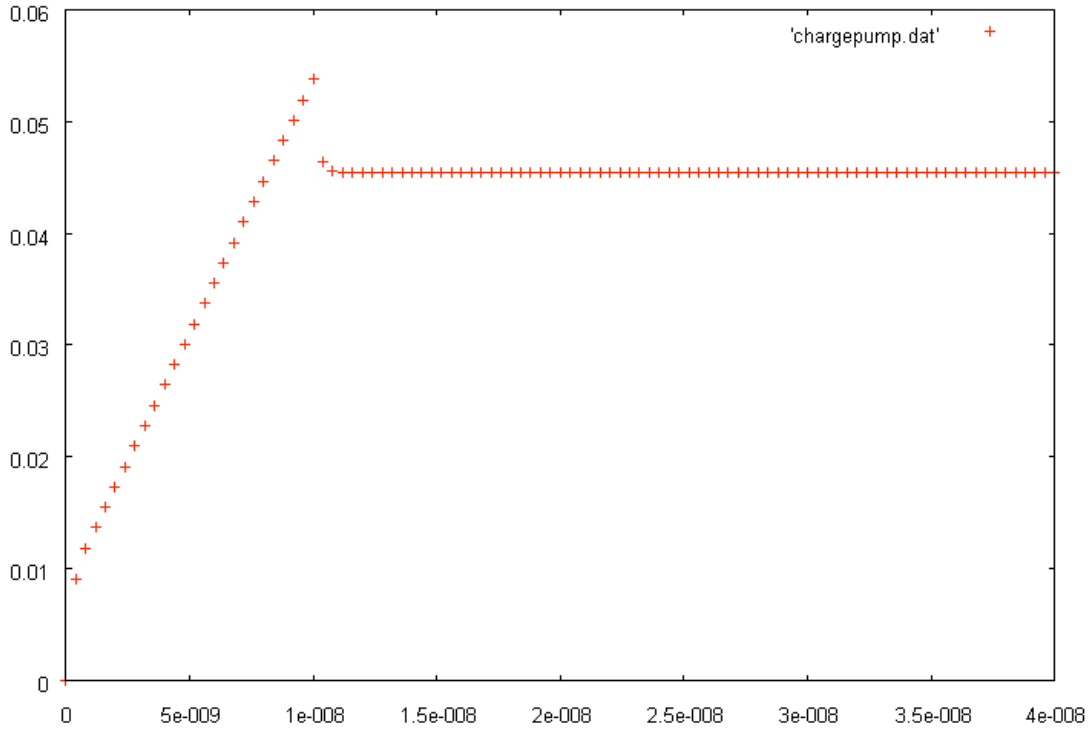

Figure 13 v(1) with C_1=2 pf and C_2=0.2 pf

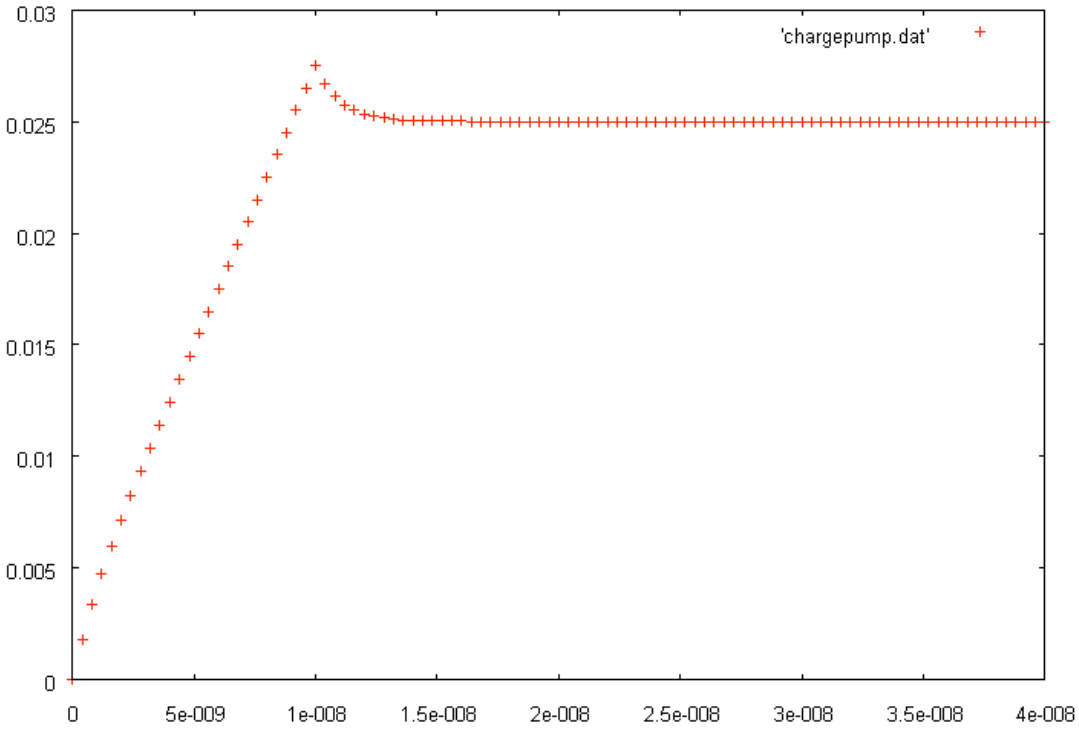

Figure 14 v(1) with C_1=2 pf and C_2=2 pf (to exaggerate smoothing)

Appendix B Charge Pump PLL Design Equations

In modeling the charge pump PLL, if we assume C1 >> C2 as is the case, and also assume that the input reference frequency is much larger than the loop bandwidth, then we can model the PLL as a continuous system (this is an approximation). We also assume that we are in the tracking mode so that phase errors are small. In this case, we have the following results:

Loop Gain and Bandwidth (Hz):

$$K = \frac{K_0 I_p R_1}{2\pi N}$$

Natural Frequency:

$$\omega_n = \sqrt{\frac{K_0 I_p}{2\pi N C_1}}$$

Damping Factor:

$$\zeta = \frac{1}{2} R_1 \sqrt{\frac{K_0 I_p C_1}{2\pi N}}$$

Note that the specification of any two of the above parameters determines the third:

$$K = 2\omega_n \zeta$$

$$\zeta = \frac{\sqrt{K\tau}}{2}$$

$$\frac{K}{\tau} = \omega_n^2$$

In the above,

$$\tau = R_1 C_1$$

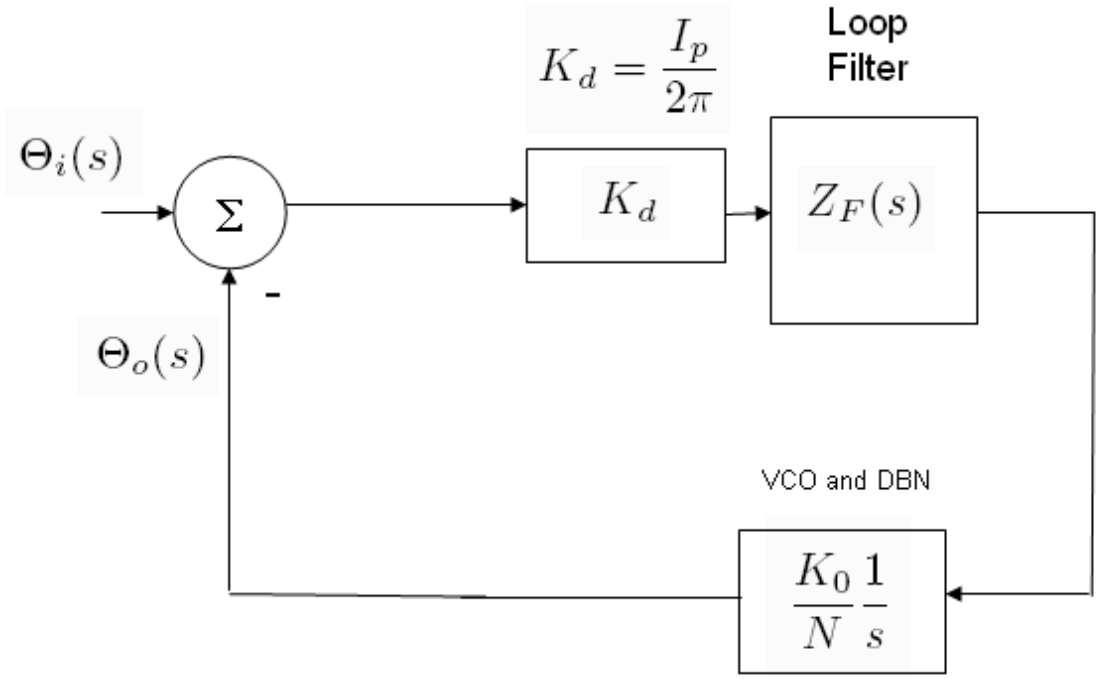

Figure 15 s-Domain Block Diagram Charge Pump PLL

Note that with the assumptions that were made above, the transfer function between the input phase $\theta_i(s)$ to the output phase $\theta_O(s)$ in the s-domain (see Figure 15) has a denominator D(s):

$$D(s) = s^2 + s\zeta\omega_n + \omega_n^2$$

Noting that the inverse Laplace transform of :

$$\frac{1}{s^2 + s\zeta\omega_n + \omega_n^2}$$

is the time domain signal:

$$e^{-\zeta\omega_n t}\sin(\sqrt{1-\zeta^2}\omega_n t)\frac{1}{\sqrt{1-\zeta^2}\omega_n}$$

We observe that the rate of convergence is related to the bandwidth K and increasing the damping factor reduces ringing.

Stability:

Now it is very important to take into consideration that the charge pump PLL is more accurately modeled in the z-domain as a sampled system with the sampling frequency determined by the input reference frequency f_i. In this case, the system can go unstable if the reference frequency is much lower than the loop bandwidth. The loop gain beyond which the system is unstable has been derived in [2]:

$$K_{stable} = \frac{1}{\frac{\pi}{2\pi f_i \tau}\left(1+\frac{\pi}{2\pi f_i \tau}\right)}$$

The issue to be concerned with here is that although in a clock synthesizer application we require a high bandwidth, the system can go unstable if the reference clock is decreased. But if the reference decreases we must increase N which also reduces the bandwidth.