Capsim Application Note

No. 6 December 199

Clock Recovery from Phase-Encoded Data

Introduction

This application note describes the simulation of a clock recovery circuit for phase-encoded data. The simulation is modelled after a circuit appearing in the Motorola MECL Device Data book (1987) as an application note on pages 6-40 to 6-42 of the MC4044 phase-frequency detector device data. The circuit consists of logic circuitry and a phase-locked loop (PLL). This simulation illustrates the modelling of a combination of analog and digital logic functions.

System Description

The top level block diagram of the system is shown in Fi 1. A *bdata* star generates a random data stream which converted to a biphase signal using *linecode*. The data shaped by convolving with a rectangular shape usir *convolve* and converting to digital 0 or 1 using *limiter*.

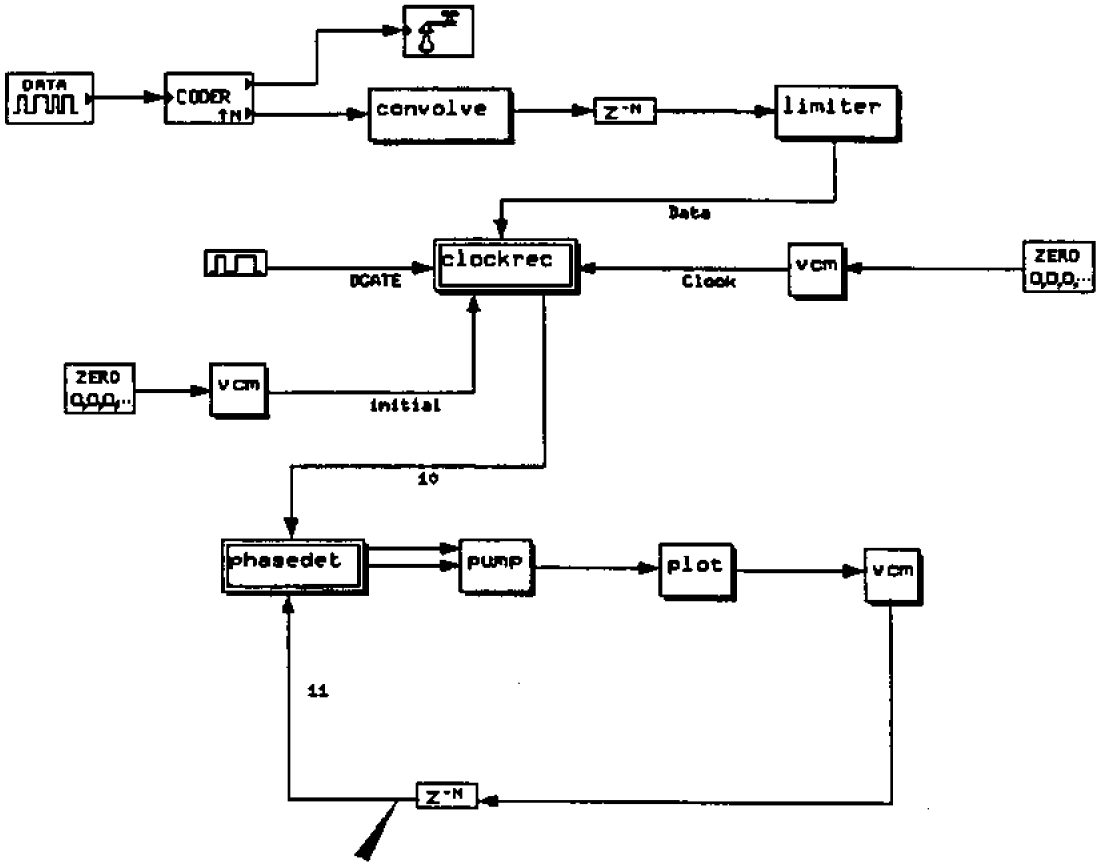
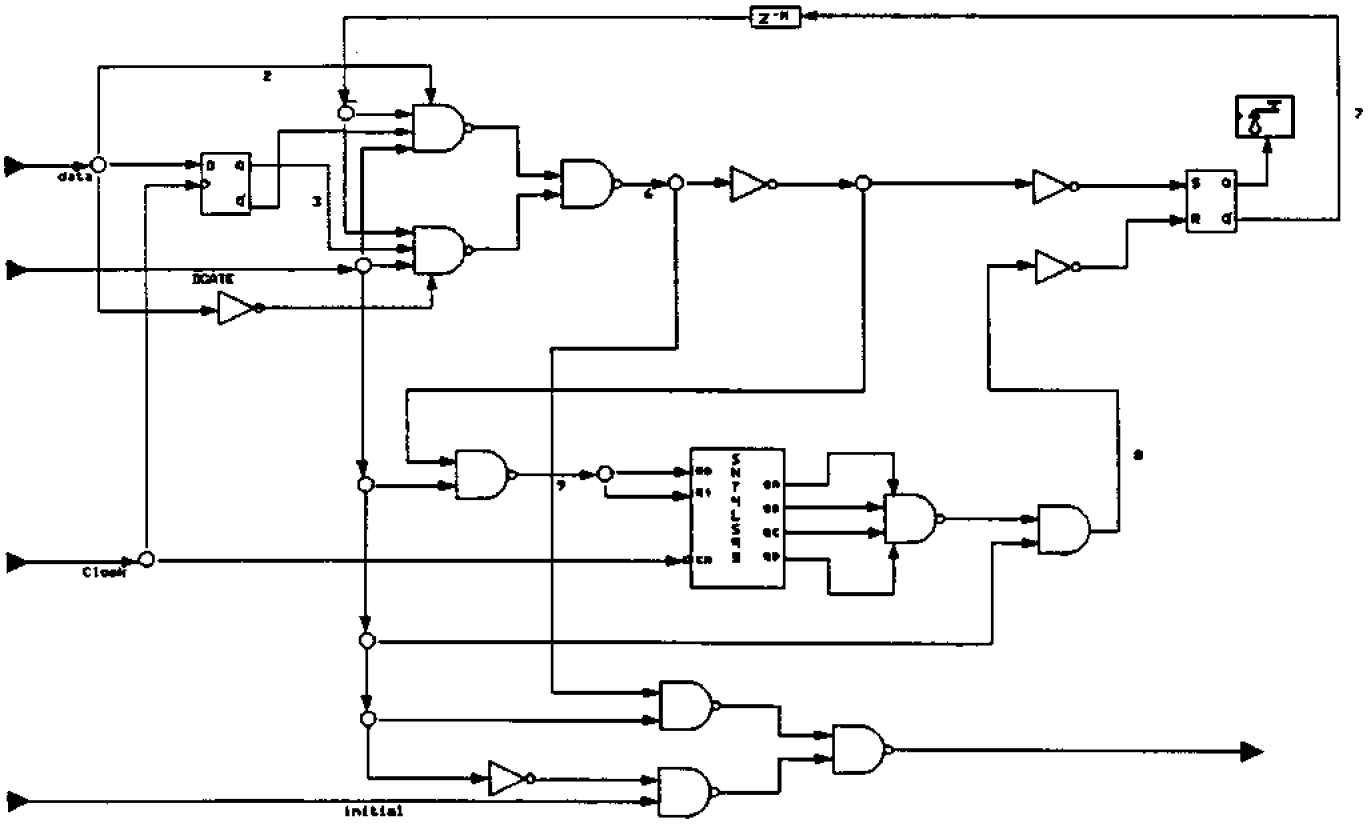


Figure 1.

A majority of the system is contained in the galaxy *clockrec* shown in Fig. 2. This logic circuitry generates a pulse at the midpoint of each data cell. The signal DGATE is used to initialize the circuitry and insure that the first transition of the data block is ignored, and is generated using *pulse*. One voltage controlled multivibrator (*vcm*) is used to provide a clock at 24 times the data rate for the galaxy. Another *vcm* operates at slightly less than the data rate which is applied to the PLL when DGATE is logic 0. This reduces the acquisition time of the PLL by providing a frequency approximately equal to the expected data rate during gaps in the data. For a detailed discription of the circuit see the MECL Device Data book.

The *SN74LS93* star is a binary counter that, along with the *srlatch*, generates a suitable signal for gating out pulses at (6) caused by phase transitions at the end of a data cell. The initial pulse at (6) sets (7) low and is combined with DGATE to reset the counter to its zero state. Subsequent *vcm* pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state results in a negative transition at (8). This causes (7) to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

The output of *clockrec* is connected to the PLL which consists of a phase-frequency detector (*phasedet*), charge pump (*pump*), *vcm*, and *delay*. The galaxy, *phasedet*, shown in Fig. 3 is a model of the detector portion of the MC4044.



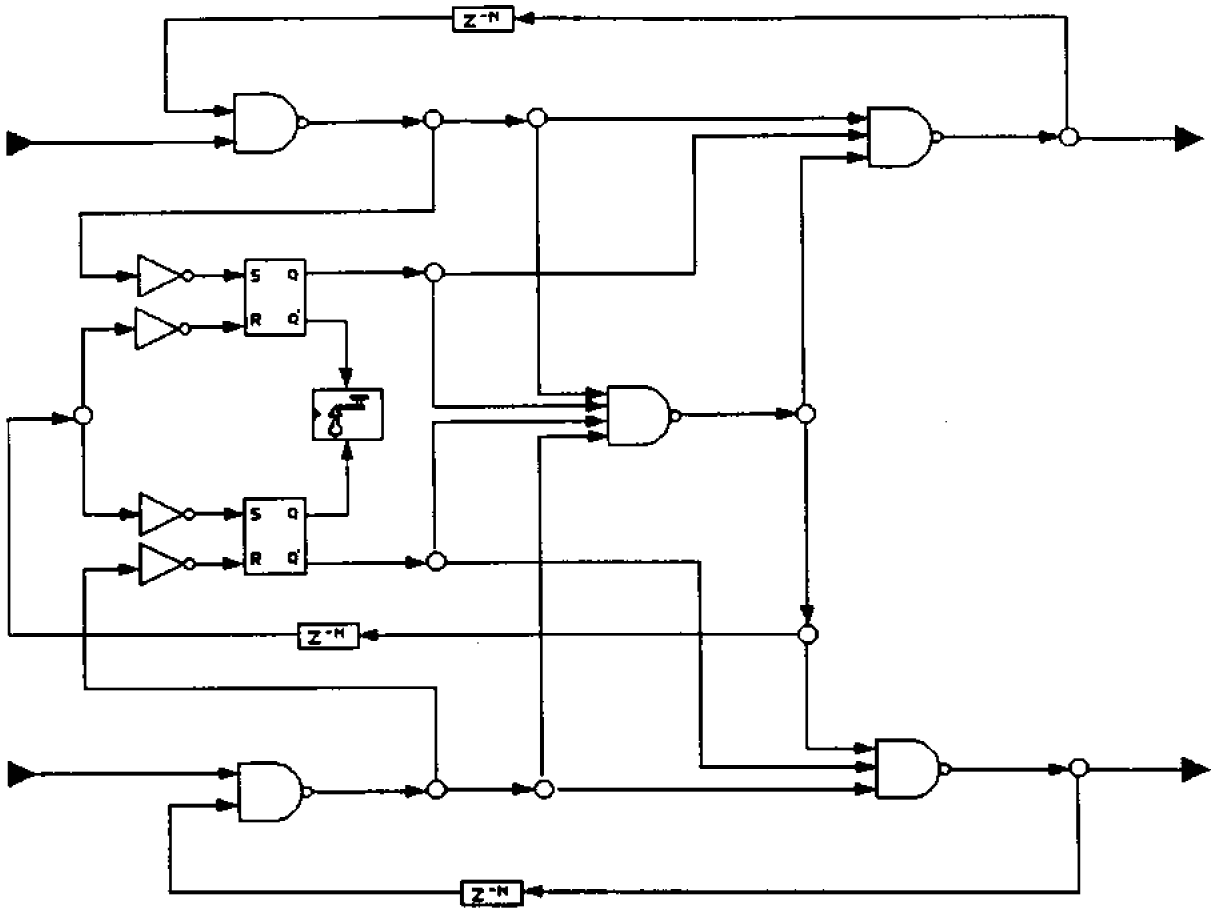


Figure 3.

The star, *pump*, is a combination of the charge pump portion of the MC4044 and the loop filter with parameters corresponding to the charge pump current and integration gain. An example of the pump output with integration gain of 0.2 and voltage step of 0.5 is shown in Fig. 4. Plots for both positive and negative phase offset of equal amplitude are shown. Note that this model produces a symmetric response about the zero phase difference point which is important in the PLL operation. A *delay* with parameter one is required in the feedback loop to provide the desired PLL response.

Simulation Results

This circuit was designed to regenerate the clock from digital data recorded on magnetic tape. The data rate is 120 KHz and the clock rate is 24 times this, or 2.88 MHz. To provide adequate resolution the sampling rate was set to 8 times the clock rate, or 23.04 MHz. Fig. 5 shows the simulation ouput after the PLL has settled (9000 sample The waveform labels correspond to the numbering used the data book and also as shown in the Capsim topolo block diagrams. This logic analyzer simulation outp compares with Fig. 33 of the data book. Notice that the PL output (11) is the clock corresponding to the input data (

The signal entering the *vcm* of the PLL is shown in Fig. for 10000 points. This corresponds to the error in the pha estimation for the PLL. Notice that the error settles afi about 9000 points. By varying the *pump* parameters t dynamics of the PLL can be controlled, such as the settli time, peak overshoot, and loop bandwidth.

Conclusion

This report illustrates the usefullness of Capsim as simulation tool for investigating the operation of a practi synchronization circuit. Furthermore, this application gi valuable insight into the dynamics of a PLL.

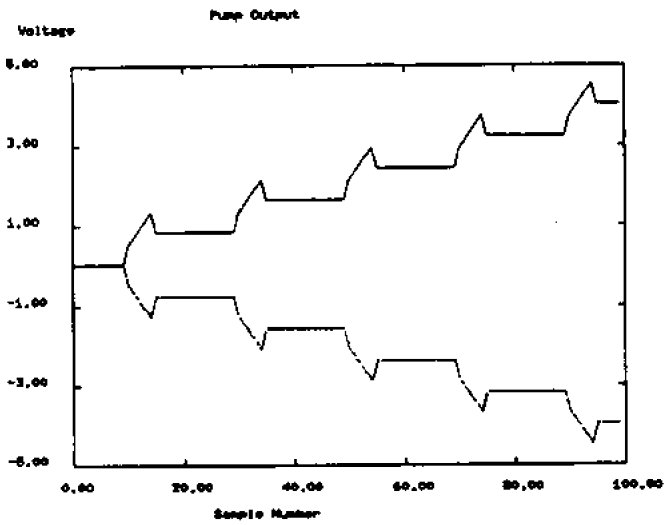


Figure 4.

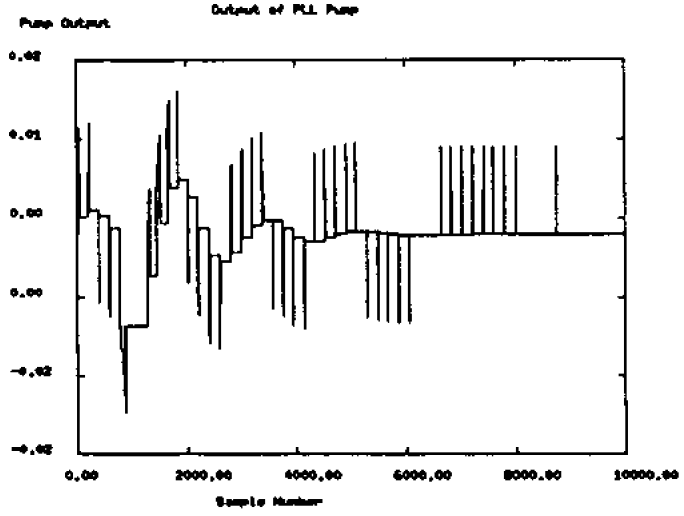


Figure 6.

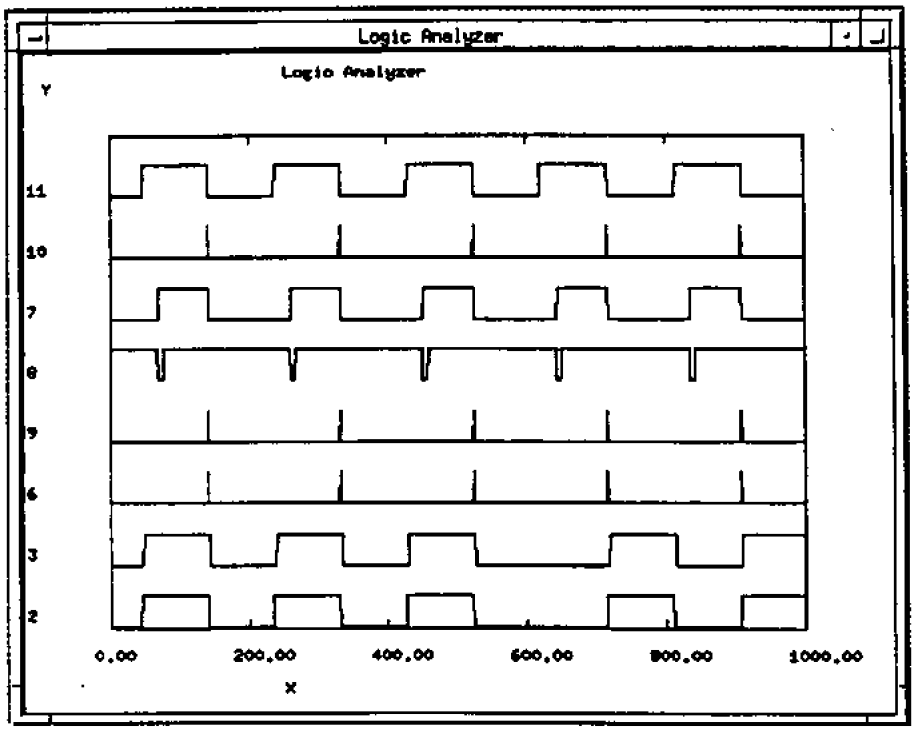


Figure 5.

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All topologies and plots in this report were produced by Capsim in PostScript.

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